## User's Graphical User Interface(GUI) for LP555x Evaluation Board PowerWise™ Technology Compliant Energy Management Unit

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## Overview

A user's graphical user interface (GUI) is provided to control LP555x evaluation boards via USB connection. The GUI for LP5551 is shown in *Figure 1* as an example. The GUI can read and write LP555x registers and send PWI commands to

program the output voltages of the switching regulators and LDOs. The GUI can also control the operation modes of LP555x, such as sleep, wakeup, shutdown and reset, by generating PWI commands. Functions and performance of the LP555x can be tested easily through the GUI.

OTH         R1 - Unused         OD	0	DO	D1	D2	D3	D4	D5	D6	D7	ADDR REGISTER
On H         Outcoment         O <t< td=""><td>DC0 00 R</td><td>C1   VDC0  </td><td>VDC1</td><td>VDC2</td><td>VDC3</td><td>VDC4</td><td>VDC5</td><td>VDC6</td><td>-8</td><td>00H R0 - Core Voltage</td></t<>	DC0 00 R	C1   VDC0	VDC1	VDC2	VDC3	VDC4	VDC5	VDC6	-8	00H R0 - Core Voltage
OH         R3         Status Register         O <tho< th=""> <tho< th=""> <tho< th=""></tho<></tho<></tho<>	00 R									01H R1 · Unused
O3H         R3 - Status Register         O3         O         C3         O         C3         O         C3         O         C3         C4         C3         C4	0 00 R V	)	0-	-0-	VDC0	VDC1	V0C2	VDC3	-0	02H B2 · V03 Vmem_ret
OSH R5         NWELL Biss         Sign         VDC4         VDC3         VDC2         VDC1         VDC0         -0         00           06H R6         PWELL Biss         Sign         VDC4         VDC3         VDC2         VDC1         VDC0         0         0         00 <t< td=""><td></td><td></td><td>-1-</td><td>-1-</td><td>-1-</td><td>-Ú-</td><td>-3-</td><td>-0-</td><td>Ĵ.</td><td>03H R3 - Status Register</td></t<>			-1-	-1-	-1-	-Ú-	-3-	-0-	Ĵ.	03H R3 - Status Register
OBH         R6         FWELL Bias         Sign         VDC4         VDC3         VDC2         VDC1         VDC0         0         0         00           07H         R7         -VD21/0 Reg	810 00 R V	rt 810	881	B12	803	B34	8115	836	Bit7	04H R4 · PWI Version
OPH         R7         VDC10         O<	-0- 00 R V	i()-	-()-	VDCO	VDC1	VDC2	VDC3	VDC4	Sign	05H R5 - NWELL Bias
O7H         R7         -VD21/0 Reg         O         VDC3         VDC2         VDC1         VDC0         O </td <td>0 00 R</td> <td>-0-</td> <td>- 0-</td> <td>VDC0</td> <td>VDC1</td> <td>VDC2</td> <td>VDC3</td> <td>VDC4</td> <td>Sign</td> <td>OSH RG · PWELL Bias</td>	0 00 R	-0-	- 0-	VDC0	VDC1	VDC2	VDC3	VDC4	Sign	OSH RG · PWELL Bias
OBH         R8 -VO1 Reg         O         VDC3         VDC2         VDC1         VDC0         O <td>0  00 R V</td> <td>յդ.</td> <td>-0-</td> <td>-0-</td> <td>VDC0</td> <td>VDC1</td> <td>VDC2</td> <td>VDC3</td> <td>-0-</td> <td>07H R7 - V021/0 Reg</td>	0  00 R V	յդ.	-0-	-0-	VDC0	VDC1	VDC2	VDC3	-0-	07H R7 - V021/0 Reg
OBH         R9         PFM//PVM Force         O         O         O         AVS Force PFMI AVS Force PFMI AVS Force PFMI DVS Force PFMI 00         O         O         O         O         O         O         O         O         AVS Force PFMI AVS Force PFMI AVS Force PFMI DVS Force PFMI 00         O <td>0 R</td> <td>J0.</td> <td>-0-</td> <td>.0.</td> <td>VDC0</td> <td>VDC1</td> <td>VDC2</td> <td>VDC3</td> <td>-0-</td> <td>09H R8 - V01 Reg</td>	0 R	J0.	-0-	.0.	VDC0	VDC1	VDC2	VDC3	-0-	09H R8 - V01 Reg
OBH         R11 - Enable         Control         O	DICE PWM 00 R	ce PFM DVS Force PWM	DVS Force PFM	AVS Force PWM	AVS Force PFM	. <u>0</u> .	-3	0.	÷.	09H R9 · PFM/PWM Force
OCH         R12 - V04 Reg         O         VDC3         VDC2         VDC1         VDC0         O<	DC0 00 R V	C1 VDC0	VDC1	VDC2	VDC3	VDC4	VDC5	VDC6	ŋ.	0AH R10 - DVS Switch Reg
00H R13 - GPO Control           PwELL I Cet_1         PwELL I Cet_0         GPO_3         GPO_2         GPO_1         GPO_0         00           0EH R14 - Reserved           GPO_3         GPO_2         GPO_1         GPO_0         00            0FH R15 - Reserved           GPO_2         GPO_1         GPO_0         00          00          00          00	Enable 00 R	Enable V03Enable	NWELL Enable	PWELL Enable	V01 Enable	VO4 Enable	DVS Enable	Û.	Ð	08H R11 - Enable Control
0EH         R14 - Reserved         00           0FH         R15 - Reserved         00           F8H         Control Input:         ENABLE           F9H         Status Output:         00           F9H         Status Output:         00           FAH         PWI Commands         Reset           Steep         Shutdown         Wakeup	0 00 R V	)	0-	-0-	VDC0	VDC1	VDC2	VDC3	8	0CH R12-V04 Reg
F8H     Control Input:     ENABLE     RESETN       F9H     Status Output:		0_1 GP0_0	GP0_1	GPO_2	GPO_3	PWELLICH_0	PWELLI CH_1	-Ð.	÷	0DH R13 - GP0 Control
F8H     Control Input:     ENABLE     RESETN       F9H     Status Output:										0EH R14 - Reserved
FAH PWI Commands Rezet Shutdown Wakeup Authenticate Synchronize	00 <u>R</u>									OFH R15-Reserved
FAH PWI Commands Reset Shutdown Wakeup Authenticate Synchronize	m elv						1	RESETN	ENABLE	FOLL Control locy &s
	00 R V			1	Asth_DK		PWBD:	112.52111	LIMOLL	
	thronize   00 R   1	nticate   Synchronize	Authenticate			Wakeup	Shutdown	Sleep	Beset	FAH PWI Commands
										-
FBH Core Votage Adjust V6V5V4V3V2V1V0		1 V0	V1	V2	V3	V4	V5	V6	÷	FBH Core Voltage Adjust _
FEH GPIO Byte A GP01 Output GP01 Output GP00 Output GP00 Output 🔘	a Gutper 00 R	Gapat GP00Gutpat	GP01 Output	GP02.0u/pu/	GP00 Output					FEH GPIO Byte A

FIGURE 1. LP5551 Evaluation Board User's GUI

## **Quick Start**

- 1. Run the GUI ('Evaluation.exe', with 'Evaluation.ini' and 'usblptio.dll' in the same folder) from the PC.
- 2. Connect the LP555x Demo Board to a PC using a USB cable.
- 3. Check authentication by clicking the 'Authenticate' button on the lower part of the GUI. Then click 'R' on the right of

the 'Auth\_OK' button to read back the authenticate result. If 'PWROK' and "Auth\_OK' are both '1' (in their depressed positions), then authentication is succeeded and the GUI is ready to control the LP555x evaluation board.

4. From the menu: Operations -> Read all, the default register values can be read from the LP555x and shown in the GUI, as shown in *Figure 2*.

ADDR REGISTER	D7	D6	D5	D4	D3	D2	D1	DO		
00H R0 · Core Voltage	-0-	VDC6	VDC5	VDC4	VDC3	VDC2	VDC1	VDC0	7F	BW
01H R1 · Unused				and the second states of the					00	BW
02H R2 · VO3 Vmem_ret	-0	VDC3	VDC2	VDC1	VDC0	-0-	0-	-0 ·	60	RW
03H R3 - Status Register	-D-	-0-	-3-	-0-	-1-	.1-	-1-	-1-	0F	RW
04H R4 · PWI Version	Bit7	836	Bit5	B34	BIG	B).2	871	Bit0	01	RW
05H R5 - NW/ELL Bias	Sign	VDC4	VDC3	VDC2	VDC1	VDC0	-0-	- <u>1</u> -	00	RW
OSH R6 · PWELL Bias	Sign	VDC4	VDC3	VDC2	VDC1	VDC0	-0 ·	-0-	00	RW
07H R7 - V021/0 Reg	-0-	VDC3	VDC2	VDC1	VDC0	-0.	-0-	.ŋ.	78	RW
09H R8 - V01 Reg	-0-	VDC3	VDC2	VDC1	VDC0	-0-	-0-	-0.	28	R W
09H R9 · PFM/PWM Force	-0-	0.	-3	0	AVS Force PFM	AVS Force PWM	DVS Force PFM	DVS Force PWM	00	
OAH R10 - DVS Switch Reg	-0-	VDC6	VDC5	VDC4	VDC3	VDC2	VDC1	VDC0	7F	RW
08H R11 - Enable Control	-0-	-0-	DVS Enable	V04 Enable	V01 Enable	PWELL Enable	NWELL Enable	V03Enable	3F	RW
0CH R12-V04 Reg	0	VDC3	VDC2	VDC1	VDC0	-0-	-0-1	-0-	78	RW
0DH R13 - GP0 Control	- <u>1</u> -	-Ö-	PWELLI CaL1	PWELLICH_0	GPO_3	GP0_2	GP0_1	GP0_0	00	RW
OEH R14 - Reserved									00	R W
OFH R15-Reserved	ENABLE	RESETN	_						[CT	1. 1996.
F9H Status Outputs		1 11202111	PWROK		Auth DK				20	R W
FAH PwI Commands _	Reset	Sleep	Shutdown	Wakeup			Authenticate	Synchronize	00	RW
FBH Core Voltage Adjust _	-0-	V6	V5	V4	V3	V2	V1	VO	7F	RW
								GP00 Gulptz	FO	

### FIGURE 2. LP5551 GUI with Default Register Values and Commands

There are a few ways to read and write to the registers through the GUI.

#### **Register Read:**

- Click button 'R' at the right of each register to read the • register value from the LP555x.
- Operations -> Read all (Ctrl+R), to read all register values.
- Operations -> Direct access, to read a single register by providing its address.
- Settings -> Register polling, when 'polling time' is not zero, all registers are read in once every 'polling time'.

### **Register Write:**

- Click button 'W' at the right of each register to write to it in LP555x.
- Operations -> Write all (Ctrl+W), to write the current values in the GUI to all registers in the LP555x.
- Operations -> Direct access, to write to a register by providing its address and value.
- Settings -> Update immediately, when checked, registers in LP555x are written whenever the buttons in the GUI are updated.

## **GUI Layout and Conventions**

### **GUI LAYOUT**

The upper half of the GUI is the register interface and the lower half is the control and PWI command interface.

From the left to the right of the GUI, as shown in Fig. 2:

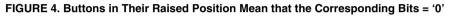
- The 1st column is the addresses for LP555x registers and control commands.
- The 2nd column shows the register names in LP555x.
- The 3rd column gives brief descriptions of registers and control commands.
- The 8 buttons in the register interface represent the 8 bits of each register. From the left to the right: MSB to LSB. Buttons in the control and PWI command interface represent each command and status.
- The two-digit HEX numbers show the contents of each register.
- The 'R' and 'W' buttons at the right end of each line are for reading from or writing to the register in the same line.

### **GUI CONVENTIONS**

In the GUI, buttons in D7 to D0 columns represent a digital bit of LP555x registers or a control command.

Buttons with grey text represent read-only or unused bits. Buttons in the depressed position show the corresponding bits are equal to '1'. For example, in Fig. 3, 'ENABLE' = '1', 'RESETN' = '1', 'PWROK' = '1' and 'Auth OK' = '1'.

F8H Control Inputs F9H Status Outputs	ENABLE RESETN	PWROK	Auth_0K	C0         R         W           28         R         W
Ittons in the raised po- ual to '0'. For example	sition show the correspo ə, in Fig. 4, 'ENABLE' =	onding bits are	on Mean that the Corresponding B	30024503 its = '1'
0', 'PWROK' = '0' and	3 'Autn_OK' = '0'.			
F8H Control Inputs F9H Status Outputs	ENABLE RESETN	PWROK	Auth_OK	00 <u>R</u> W 00 <u>R</u> W
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# Register Interface (Direct Read and Write)

A register control established through PWI interface allows users to directly access to the LP555x registers. A set of up to sixteen 8-bit registers in the PWI slave are supported by the PWI standard. By reading and writing through the GUI, output voltages of switching regulators, LDOs and others, such as P- and N- well biasing voltages, can be controlled. Please refer to the LP555x data sheets for the details related to the coding of the registers at www.national.com and powerwise.national.com.

## **Control and PWI command interface**

The lower part of the GUI is for hardware resets, enables and direct PWI commands, as shown in Fig. 2. Please refer to PowerWise Interface Specification for the details of PWI standard at pwistandard.org.

- Control Inputs
  - RESETN: controls hardware reset pin, active low, default = 1.
  - ENABLE: controls hardware enable pin, active high, default = 1.
- Status Outputs:
  - PWROK: if the evaluation board is correctly powered, a '1' will be showed in this button, otherwise '0'.
  - Auth\_OK: if authentication is successful after clicking 'Authenticate' button, a '1' will be returned when the button 'R' on the right of this row is clicked, otherwise, '0'.
- PWI Commands:

Please deselect a command after it is sent

- Reset: writing the reset command will initialize the PWI slave and set all the slave registers to default.
- Sleep: writing the sleep command to the PWI slave activates the Sleep-mode. In the sleep mode, the core voltage is 0V, and the LDO3 output (memory voltage) will be controlled by its retention value (R2). Other voltages retain their programmed values.
- Shutdown: writing the shutdown command will cause the PWI slave to switch off all regulators, thus causing

all output voltages to go to zero. Toggle hardware 'ENABLE' or 'RESETN' to activate the outputs.

- Wakeup: this command allows the PWI slave to move from sleep-mode to active-mode. The core voltage returns to the default value and LDO3 tracks the core voltage.
- Authenticate: the authenticate command is a nineframe sequence consisting of the Authenticatecommand followed by four challenge/response frame sequences. If authentication succeeds, a '1' will be returned at 'Auth\_OK' after reading the status output.
- Synchronize: this command synchronizes the master and the slave. The master sends a stream of '1's and forces the slave to resynchronize to the stop bit ('0') of the command.
- Core Voltage Adjust:
- Adjust core voltage directly. This command has the same effect as executing a register write to the register R0. However, the core voltage adjustment frame command only requires one frame to write to the R0, while a register write command needs two frames to execute.

Note that both of the core voltage adjustment command and a register write to R0 can change the content of register R0. However, the content shown in the GUI does not update until a register read is performed.

### Menus

Menus of the GUI provide various operations and settings of the GUI.

- File
  - Open profile: open a profile to overwrite the current settings in the GUI. A dialog shown in Fig. 5 will pop up, providing a choice of overwriting register contents in the LP555x or not.

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### FIGURE 5. Confirm Overwriting Registers in LP555x

- Save profile: save the current settings as a profile;
- Exit: close the GUI
- Operations
  - Write all: write all the current settings in the GUI to the registers in LP555x;
  - Read all: read all the register current values from the LP555x;
  - Set default all: set all the values in the GUI to default (please refer to the LP555x data sheets for the default value settings). A dialog shown in Fig. 5 provides choice of overwriting register contents in the LP555x or not.
  - Direct access: read from or write to an address directly. As shown in Fig. 6, a register can be written directly in the 'write' section, while a register can be read in the 'read' section.

Wile Address (hex) 0	Dala (hex) 0 🛟 Data (bin)	Wike
Read Address (hex) DO	Data (hcx) 00 Data (bin)	Read
	Close	

**FIGURE 6. Direct Access to Registers** 

 Output voltages: as shown in Fig. 7, 16 outputs of the onboard ADC can be shown. The first row shows the ADC data (hex format) and the second row shows the corresponding voltages.

DVS SW 17B 1.22	AVS SW 175 1.20	NWELL 173 1.20	LDO1 17A 1.22	LD 04 3FF 3.30	LD02 3FF 3.30	LD03 17F 1.23	000
000	000	000	000	000	000	000	000
			(Read)	Close			

- Settings
  - Update immediately: when checked, registers in LP555x are written whenever updated in the GUI.
  - Register polling: a polling time can be set in the dialog shown in Fig. 8. When the polling time is not zero, 'read all' is performed once every 'polling time'; when the bar is set at 'polling is not available', auto-polling is stopped.

Direct Acces Wile	Dala (hex)	2
Address (hex)	0 🖕 Data (bin)	Wite
Read Address (hex)	Data (hex) [00 Data (bin)	Read

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### FIGURE 8. Register Polling Interval

• History: previous register read and write actions are listed in the history window, as shown in Fig. 9.

Nistory	- D X
(Clear	
Read 00 - 7F	^
Read 02 - 60	
Read 03 · OF	
Read 04 - 01	
Read 05 - 00	
Read 06 - 00	
Read 07 - 78	
Read 08 - 28	-
Read 03 - 00	10
Read 0A - 7F	
Read 08 - 3F	
Read 0C - 78	
Read 00 · 00 Read F8 · C1	
Read F3 - C1 Read F3 - 20	
Read FA - 00	
Read FB - 7F	
neauro - /r	~

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**FIGURE 9. History Window** 

Help: version information, website and help email address.

# Notes

AN-1653

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AN-1653

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